AMENDMENT TO THE DRAWINGS

Attached hereto please find an "Annotated Marked-Up Drawing" sheet Figure 1. The revision to this figure changes the direction of the signal arrows between reference blocks 130 and 140, as well as reference blocks 140 and 150. Accordingly, a replacement sheet bearing changes to signal arrows in Figure 1 is also enclosed.

REMARKS

Reconsideration of the application is respectfully requested.

For the Examiner's convenience and reference, Applicants' remarks are presented in the order in which the corresponding issues were raised in the Office Action.

Drawings

The drawings were objected to as having reference characters "150" and "24" as both being used to designate a Highly Linear Phase Interpolator (HLPI). Although the Office Action refers to 37 C.F.R. §1.84(p)(4) as the relevant patent rule in this case, Applicants respectfully submit that the use of different reference characters as referring to the HLPI is clearly in connection with different figures and different embodiments of the invention and, accordingly, does not create any confusion to the reader. For instance, HLPI 150 is described in connection with Figure 1, whereas HLPI 240 is described with reference to Figure 2. These may be viewed as different embodiments of an interpolator. There is also another HLPI 800, shown and described in connection with Figure 8. The text of the Detailed Description does not confuse between the different reference numbers but rather describes each instance of the HLPI in the context of its own figure consistently. This also occurs with other components in the diagram that would appear to deserve the same reference. Given the manner in which these components are consistently described in connection with their respective figures, no change is believed to be necessary to further clarify the drawings.

The Applicants, however, thank the Examiner for recognizing several mistakes in Figure 1 concerning the input and output signals to the phase controller 140. These have been corrected in Figure 1 so as to remain consistent with the other figures and the text of the Detailed Description.

Although the Examiner also objected to the lack of input and output arrows in certain of the figures, namely Figure 2, for example, and the components inside the HLPI 240, it is respectfully submitted that when viewed in light of the text, the input

and output relationship between the different components shown is clear and does not require arrows.

Regarding paragraph "e." at the bottom of page 2 of the Office Action, where output and input arrows were requested for the components in block 240, as explained above, this is not necessary given that the components can be interpreted together with their respective textual descriptions in the Detailed Description.

Turning now to page 3 of the Office Action, the Examiner requested that in Figure 5 the label for the voltage controller 500 be changed to phase controller. This is not believed to be necessary to understand the different embodiments of the invention, because the Detailed Description indicates that the voltage controller 500 may be an embodiment of a phase controller that adjusts a voltage amplitude of an interpolated control signal (see Applicants' Specification as filed, paragraph [0047]).

Regarding the objection to Figure 6 and the labels VC A and VC B not being shown in Figure 5, here, once again, it is respectfully submitted that the lines that connect the different blocks are not necessarily pointing to any particular input or output, but rather indicate some form of communication or connection occurring between the two different blocks. Once again, the Detailed Description, in particular paragraph [0060], clarifies that Figure 6 is an embodiment of certain circuitry that substantially maintains a common mode voltage between two control signals, VC A and VC B that are output by the voltage controller 500. It is not necessary to explicitly indicate such control signals also in Figure 5, because the corresponding Detailed Description adequately describes the relationship between the two figures.

Finally, regarding item "j." on page 3 of the Office Action, the Examiner there requested that certain labels be changed in Figures 2 and 8 (*e.g.*, changing "phase controller" in Figure 2 to "voltage controller" to match the label found in Figure 8). Once again, Applicants respectfully disagree, because the phase controller shown in Figure 2 is not necessarily the same as the voltage controller shown in Figure 8. The voltage controller is an example phase controller.

Claim Rejections Under 35 U.S.C. §1.112

In this section, claim 5 stands rejected as being not enabled because it recites *degenerative mesh circuitry* that is allegedly not clearly recited in that claim. However, in response to the Examiner's questions, namely is the degenerative mesh circuitry coupled between the first and second circuitry found in the phase control circuit, and whether the degenerative mesh circuitry is part of an amplifier comprising the first and second circuitry, as well as the degenerative mesh circuitry itself, the answer is yes to both questions. This has been made clear in this amendment, where claim 24 has been amended with the relevant language. Note that the degenerative mesh circuitry is part of an amplifier that comprises the first circuit, the second circuit, and the degenerative mesh circuitry itself. As an example, the Examiner's attention is directed to Figures 8 and 9. In Figure 8, the degenerative mesh is shown as being coupled between phase control circuitry 812 and phase control circuitry 822 (Figure 8). In Figure 9, the degenerative mesh 950 is shown as a network of resistors that connect the source nodes of different phase control circuitry 912, 922, 932, 942. The *amplifier* in this case, has phase circuitry 912, 922 with inputs 918, 928. The outputs of this *amplifier* may be I1 bias and I2 bias that are used by the differential current-steering mechanisms 810, 820 (see Figure 8). See also the relevant portion of the Detailed Description, at paragraph [0074]. In view of the foregoing therefore, it is believed that the language concerning the *degenerative mesh circuitry* that has been added to claim 24 is adequately supported and enabled by the Specification as filed.

Claim Rejections Under 35 U.S.C. §102

Independent claim 1 stands rejected as being anticipated by U.S. Patent 6,380,783 to Chao, et al. ("Chao"). Applicants' respectfully disagree with the rejection for the following reasons.

Claim 1 as originally filed recites an apparatus in which interpolator circuitry is to proportion the amplitude contributions of reference clock phases, and output circuitry is to generate a phase of an interpolated clock signal with a substantially analog transition, based upon a combination of the amplitude contributions. In addition, phase control circuitry is to adjust a proportion of the amplitude contributions

based upon an interrelated control signal. Such an apparatus allows one to create phase change resolutions as small as needed, without increased circuit complexity. This is in contrast to the technique in Chao which uses discrete output steps whose granularity is a function of a digital to analog converter (DAC), that is increased DAC complexity.

In Chao, the multi-phase generation system has a weighted bias current generation block 16 (see Figures 1 and 4), which are binary weighted. The input selection bits D 34 are from a phase selection controller (not shown) which controls the amount of current present at the output nodes of the weighted bias current block 16. [Chao, col. 5, lines 6-17] The weighted currents IA and IB from the output nodes of the weighted bias current generation block 16 are used to increase/decrease the voltage present at the interpolator output nodes 70, 72 (see Figure 5). The voltage at these output nodes are provided to a comparator 20, whose output in turn is capable of the multiple phases as shown in Figure 7, depending upon the relative weighting of IA and IB.

In Chao, to increase the phase change resolution, the complexity of the current generation block 16 needs to be increased so as to provide smaller amounts of current steps to IA and IB. In addition, a phase change occurs in terms of a discrete output step, directly resulting from the switching of the current feeding transistors in the current generation block 16 (see Figure 4). There is no indication in Chao that such a change results in the phase change of an interpolated clock signal *with a substantially analog transition*. Accordingly, claim 1 as filed is not anticipated by Chao.

Nevertheless, claim 1 has been amended (with subject matter taken from dependent claim 25, which was indicated as being allowable) to recite a particular embodiment of the invention in which *degenerative mesh circuitry is coupled with the phase control circuitry to determine proportions of a bias current based upon a substantially differential portion of the interrelated control signal and another control signal.* This limitation was originally in dependent claim 4, now canceled, which was indicated in the Office Action as being directed to allowable subject matter. Accordingly, claim 1 as amended here, is believed to be in condition for allowance.

Claim Rejections Under 35 U.S.C. §103

The next independent claim, claim 17, stands rejected as being obvious in view of Chao and U.S. Patent No. 6,509,773 issued to Buchwald ("Buchwald"). Once again, Applicants respectfully disagree with the rejection.

Claim 17 is directed to a method in which an interrelated control signal associated with a first phase and a second phase of a reference clock signal is received. An amplitude contribution of the first phase and that of the second phase is proportioned, based upon the control signal. The amplitude contributions are combined based on the proportioning, to generate a phase of an interpolated clock signal with a substantially analog transition. In other words, when changing from one phase to another phase, the interpolated clock signal exhibits a substantially analog transition. See for instance, the Specification as filed, paragraph [0015] describing an embodiment which includes a phase controller 140 designed to bound the voltages or amplitudes of the interrelated control signals 146 to amplitudes within a substantially linear region of a transfer characteristic for the highly linear phase interpolator 150. Chao, however, does not teach or suggest any issues regarding the linearity of the phase interpolator.

In addition, claim 17 has been amended to refer to the interrelated control signals as a ramping voltage signal that is associated with the first and second phases of the reference clock signals. Although in Chao, the voltage at the output nodes 70, 72 are ramping voltage signals, they are not the *interrelated ramping control voltage signals that are associated with a first phase and a second phase of the reference clock signal.* Chao does not work by *proportioning an amplitude contribution of the first phase and the second phase, based upon the interrelated ramping control voltage signal.* Rather, the weight associated with each phase clock_a and clock_b in Chao is provided by IA and IB, which are not interrelated ramping voltage control signals. Applicants also respectfully submit that it would not have been obvious to modify, for example, the circuit in Figure 5 of Chao, into one where *amplitude contributions of the first phase and of the second phase of the reference clock signal are proportioned based upon the interrelated ramping control voltage signal.*

For all of the above reasons, Applicants respectfully submit that claim 17 is not anticipated or obvious in view of Chao.

Turning now to independent claim 24, this claim also stands rejected as being obvious in view of Chao and Buchwald. Applicants respectfully disagree that claim 24 as filed is anticipated or obvious, for at least the reasons given above in support of claim 1, including the observation that neither Chao or Buchwald teach or suggest a phase interpolator in which a phase of an interpolated clock signal is generated with a substantially analog transition. Nevertheless, claim 24 has been amended to recite *degenerative mesh circuitry that is coupled between different circuits of the phase control circuitry to degenerate an amplifier that comprises the first circuit, the second circuit, and the degenerative mesh circuitry itself.* The Office Action does not indicate where such a phase interpolator is taught or suggested in the cited art references. Accordingly, claim 24 as amended is also believed to be in condition for allowance.

New claim 31 is closely based on originally filed dependent claim 3 (including subject matter from its base claim 1 and intermediate claim 2). Although Chao discloses a weighted bias current generator 16 in Figure 4, that circuit provides fractions of the total current using a purely current-summing circuit, consisting of on/off transistors 42-48 each of which provides a set, discrete fraction of the total current. That does not teach or suggest using *degenerative mesh circuitry that works with phase control circuitry to apportion a static bias current based upon an interrelated control signal.*

Any dependent claims not mentioned above are submitted as not being anticipated or obvious, for at least the same reasons given above in support of their base claims.

CONCLUSION

In sum, a good faith attempt has been made to explain why the rejection of the claims is improper, and how the claims are believed to be in condition for allowance. A Notice of Allowance referring to claims 1, 6-24, 26-27, and 31-37, as amended here, is therefore respectfully requested to issue at the earliest possible date.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR, & ZAFMAN LLP

Dated: March 6, 2006

By _____
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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, Post Office Box 1450, Alexandria, Virginia 22313-1450 on March 6, 2006.

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Margaux Rodriguez *March 6, 2006*

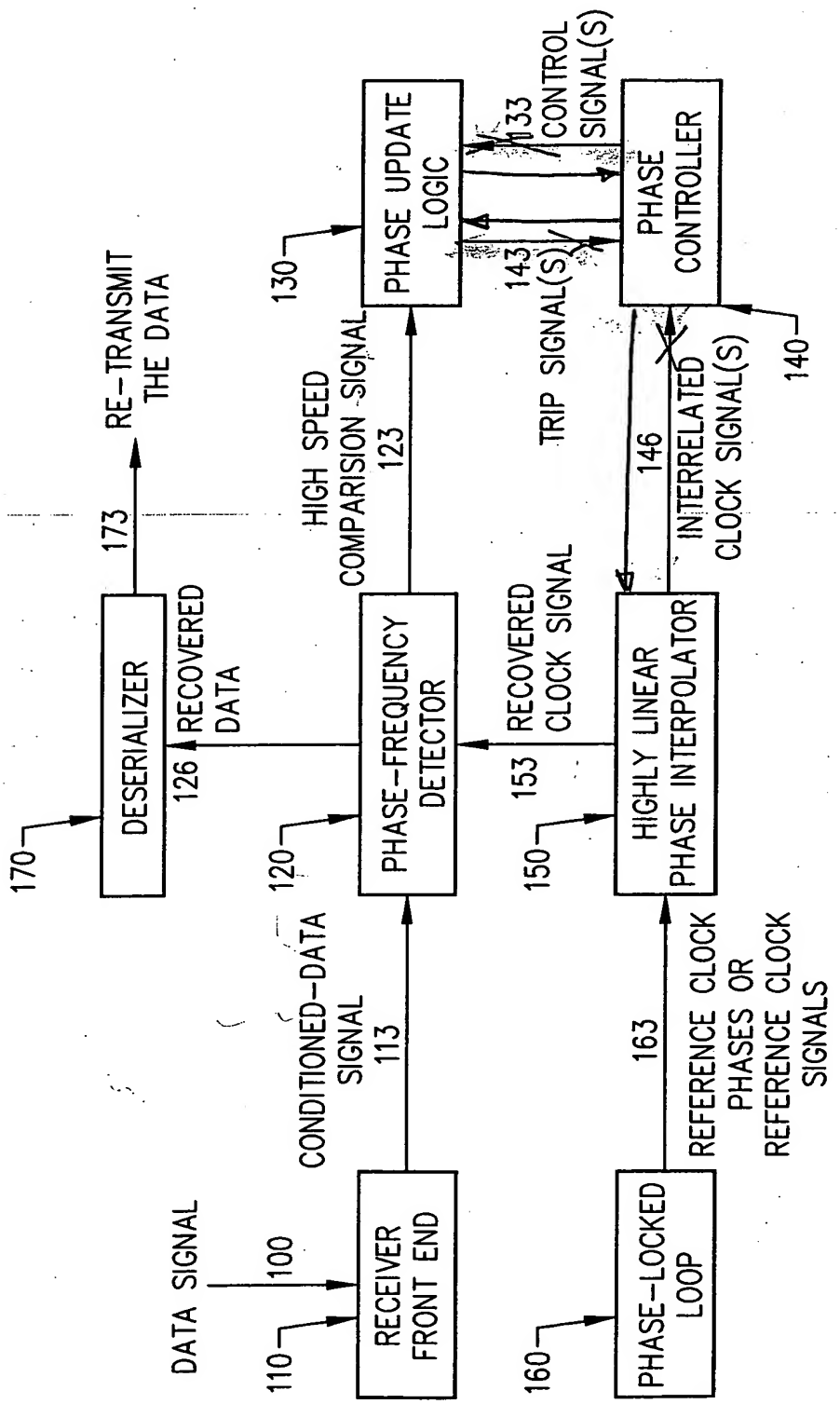

FIGURE 1